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Grid Connected Single-Phase Multilevel Inverter

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Abstract: In the microgid system, the distributed energy resource (DER) based inverters are usually adopted. Multilevel inverters have been attracting in favour of academia as well as industry in the recent decade for high power and medium voltage energy control and its multilevel concept is used to decrease the THD in the output waveform without decreasing the inverter power output and it also offer high power capability, lower commutation losses and less stress on semiconductor switches. The inverter topology in this paper is a five-level grid connected inverter having the ability to produce minimum THD with reduced number of switches and reduction in space utilization with simple control logic. The five-level inverter requires only six switches instead of eight required in the CCHB inverter. In addition, two active switches are operated at the line frequency. The most attractive feature of this proposed topology is that it requires only two carriers for developing the multilevel output; hence the control logic is simple. The inverter is simulated for both off-grid and on-grid applications. The inverter current THD is obtained as 1.74% which is less than 5.0% and compatible with the THD utility standards.

Keywords: Distributed Energy Resources (DER); Photovoltaic (PV); DC/DC converter; Conventional Cascade H-Bridge Multilevel Inverter (CCHB).

I. INTRODUCTION

Nowadays, multilevel inverters have become more attractive for researchers due to their advantages over conventional three-level pulse width modulation (PWM) inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower THD [1], however the total number of the power electronic elements used is increased as the number of levels increased. Basically, renewable energy sources for grid connected applications are increased due to the world energy crisis. Injecting power to the utility must meet the world harmonic standards. Therefore, single phase MLIs become a good solution for those applications. Furthermore, in recent years, an industrial applications and utility application require medium voltage and high power levels.

MLIs [1] give the ability of dealing with this high power level due to its voltage staircase waveform as the voltage stress on the semiconductor components is lower. Therefore, low voltage rate switches can be utilized in a multilevel inverter. However, one of the most particular disadvantages of MLI is the large number of the required power semiconductor switches; each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Designers are now paying more attention to save electric energy by reducing the harmonics. The main objective of this work is to select the best multilevel inverter topology with less number of switches, smaller filter size and improved output waveform with low THD. For delivering premium electric power in terms of high efficiency, reliability, and power quality, integrating interface converters of DERs such as photovoltaic (PV), wind power, micro turbines, and fuel cells into the micro grid system has become a critical issue in recent years. So a detailed study on various topologies was carried out and cascade H-bridge multilevel inverter topology is found to be more efficient among all the other topologies.

The reduction in THD [2] of the inverter output provides wide applications in power quality enhancement devices and to drive sensitive loads. Modifications in the cascaded H-Bridge configuration have recently become very popular in high power AC supplies and adjustable-speed drive applications. Reduction in number of semiconductor devices will reduce the switching losses and switching complexities and therefore the system is ideal for residential and industrial applications. Various converter topologies [3] have been developed for DERs that demonstrate effective power flow control performance either in grid-connected or stand-alone operation.
Among them, the solutions that employ high-frequency transformers or make no use of transformers at all have been investigated to reduce size, weight, and expense. In order to get a multilevel output, multiwinding transformer [4] is a better solution and it is similar to the cascaded H-bridge topology, but the outputs of the isolation transformers are cascaded instead of directly cascading the H-bridge outputs. As a result, only one dc source is required. In practice, these inverters have been proved to be robust and reliable. One disadvantage of this topology is the fact that it requires several low-frequency transformers.

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Other variations of the Cascade H-Bridge [4] requires only one dc source. This topology is simple, but losses in additional rectifier diodes can be significant, and it does not support a bidirectional power flow. The topology can be very efficient if soft-switching dc/dc converters are used. On the other hand, this topology is based on high-frequency switching, and inherent benefits of low-frequency switching are lost. The multiple-source topology [4], uses several isolated dc sources to produce a rectified multilevel waveform, which is then converted into an ac voltage. In practice, the multiple-source topology is one of the most efficient multilevel topologies currently available. It has been found to be very efficient, robust, and reliable.

The disadvantage of this topology is the fact that it requires several isolated dc sources and does not provide input–output isolation. The multi-winding-transformer topology [4] can be considered as a variation of the multiple-source topology. It also requires only a single dc input, which is achieved using a multi-winding line-frequency transformer. It provides input-output isolation, and because it employs only one transformer, high efficiency can be achieved. The major disadvantage is the relatively high number of switches presented in the output stage.

The multi-string multilevel inverter topology [5] that requires only six active switches instead of the eight required in the conventional cascaded H-bridge (CCHB) multilevel inverter. In addition, among them, two active switches are operated at the line frequency. In order to improve the conversion efficiency of conventional boost converters, a high step-up converter is also introduced as a front-end stage to stabilize the output dc voltage of each DER modules for use with the simplified multilevel inverter. Also the studieded inverter has only six switches and no power diodes compared with five switches and four power diodes presented in [6], or six switches and two main power diodes presented in [7], or eight switches as in [8].

II. GRID CONNECTED SINGLE PHASE MULTI-LEVEL INVERTER

This topology [14] has a new grid-connected multi-level inverter not only with very low total harmonic distortion (THD) but also with less power electronics components. Moreover, this topology consists of a single-phase five-level PWM inverter with less number of power elements and hence less gate drive circuits in addition to less circuit layout complexity. PWM switching technique has been proposed based on reducing switching losses and the harmonic contents.

. The studied multi-level inverter is shown in Fig.1. Its output voltage has the following five levels: Zero, +Vdc, +2Vdc, −Vdc, and −2Vdc. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two carrier signals to generate PWM signals for the switches. Some switches operate at fundamental frequency and others operate at switching frequency. The powerful merit of this inverter is that the inverter has less number of elements compared with others single-phase inverter found in the literature. To increase the number of levels of the output voltage the number of cell (Cell-1) is repeated for each additional level [9]-[11].

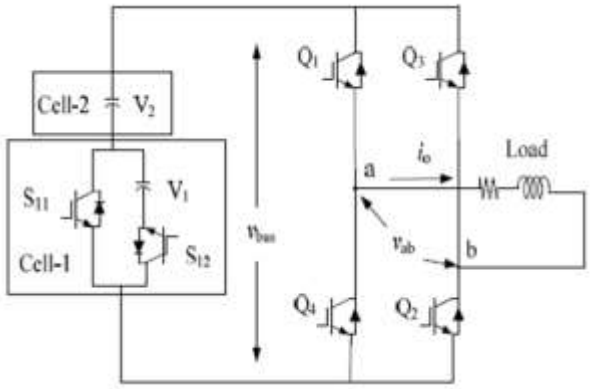

Fig.1 Studied Single-Phase Five-level Inverter [14]

Also the studied inverter has only six switches and no power diodes compared with other topologies having five switches and four power diodes or six switches and two main power diodes or eight switches as found in the literature for a five-level output. In order to generate the 5 levels, the number of the cascaded cell required is two cells (Cell-1 & Cell-2).One cell is equipped with two switches with the dc source while the other cell is only a dc source as shown in Fig.1. The load output voltage Vab will have five states 2Vdc, Vdc, 0, -Vdc 2Vdc. The states of the switches have been summarized in Table 1.

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III.DESIGN AND MODELLING OF GRID CONNECTED FIVE-LEVEL INVERTER

The PWM switching technique [12]-[13] for the single-phase five-level inverter is basically depending on generating gate signals by comparing rectified reference waveform with two in-phase triangle carriers having same frequency, same peak-to-peak, but different offset voltages. The switching pattern of the single-phase five level inverter is based on the Phase Disposition PWM technique. The intersection points between carrier A and carrier B with the reference waveform decide the inverter output voltage level. Switching states for a five-level output are illustrated in Table1.

TABLE I SWITCHING STATES FOR A FIVE LEVEL OUTPUT

Vab	Switching States					
	Q1	Q2	Q3	Q4	S11	S12
+2Vdc	ON	ON	OFF	OFF	OFF	ON
+Vdc	ON	ON	OFF	OFF	ON	OFF
0	ON	OFF	ON	OFF	OFF	OFF
	OFF	ON	OFF	ON	OFF	OFF
-Vdc	OFF	OFF	ON	ON	ON	OFF
-2Vdc	OFF	OFF	ON	ON	OFF	ON

The first level of the inverter output voltage Vdc is generated at the intersection points of reference waveform and the lower carrier signal (carrier A), whereas the second level of the output voltage 2Vdc is generated at the intersection points of the reference voltage waveform and the upper carrier signal (carrier B). The positive half-cycle of the reference voltage waveform is responsible for generating the positive dc voltage levels (Vdc and 2Vdc) in the output voltage, whereas the rectified half-cycle is responsible for generating the negative dc voltage levels (-Vdc and -2Vdc). According to the reference voltage, the intersection with the carrier may happen with the lower carrier only resulting in modulation index between zero and 0.5, or with both carrier signals resulting in modulation index between 0.5 and 1. Therefore, if the modulation index is less than or equals 0.5, the output voltage of the inverter will have only three levels (Vdc, 0, and -Vdc). On the other hand, if the modulation index is more than 0.5, the output voltage of the inverter will have five levels (±2Vdc, ±Vdc, 0,). According to the amplitude of the reference voltage, its period can be divided into five intervals based on four modes (Mode A, Mode B, Mode C, and Mode D). Based on the related displacement phase angles (θ1, θ2, θ3 and θ4), the operational modes can be defined as follows [14]:

$$\left.\begin{array}{l}\text{Mode A, } 0 < wt \le \Theta_1,\ \Theta_2 < wt \le \prod \\ \text{Mode B, } \Theta_1 < wt \le \Theta_2 \\ \text{Mode C, } \prod < wt \le \Theta_3,\ \Theta_4 < wt \le 2\prod \\ \text{Mode 4, } \Theta_3 < wt \le \Theta_4\end{array}\right\} \quad (1)$$

The modulation index (MI) of the studied single-phase five-level inverter is defined as follows:

$$MI = A_M / 2A_C \quad (2)$$

where A_M is the peak value of the reference modulating waveform, and A_C is the peak-to-peak value of the carrier. Also, the frequency ratio (mf) is defined as follows:

$$m_f = f_c / f_m \quad (3)$$

where fc is the frequency of the carrier signals, and fm is the frequency of the modulating signal. According to the intersections between the modulation waveform and the carrier signals, the period of the reference voltage (2π) is divided into six time intervals. The signals C_A and C_B, result from comparing the modulation waveform with the lower and upper triangle carriers, respectively. The gate signals of the proposed inverter switches can be calculated based on the resultant signals C_A and C_B in addition to the six time intervals (P1, P2, P3, P4, P5 and P6). The resultant gate signals of the inverter six switches can be formulated as follows:

$$\left.\begin{array}{l}Q1 = P1 + P2 + P3 \\ Q2 = ((P1 + P2 + P3).\ C_A) + ((P4 + P6).\ C`_A) \\ Q3 = ((P1 + P3).\ C`_A) + ((P4 + P5 + P6).\ C_A) \\ Q4 = P4 + P5 + P6 \\ S11 = ((P1 + P3 + P4 + P6).\ C_A) + ((P2 + P5).\ C`_B) \\ S12 = (P2+P5).C_B\end{array}\right\} \quad (4)$$

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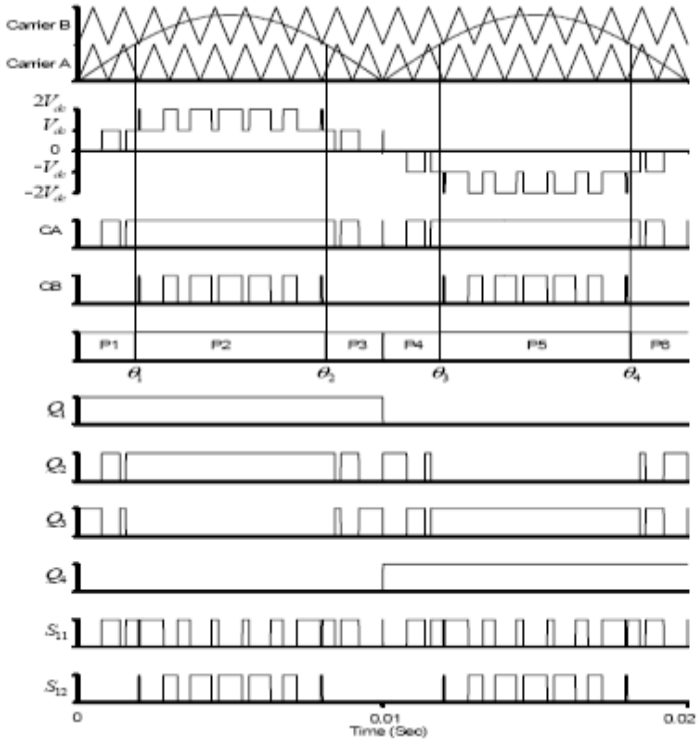

Fig. 2. Required PWM Technique for the Studied Single-Phase Five-Level Inverter [14]

is clear from (4) and Fig.2 that the inverter power switches (Q1 and Q4) are complementary switches operating at the fundamental line frequency. Also, switches (S11 and S12) cannot switch ON simultaneously. However, their switching signals are decided based on (4) and operating at switching frequency. Moreover, the power switches (Q2 and Q3) are complementary switches operating at switching frequency. The load output voltage Vab will have five states 2Vdc, Vdc, 0, -Vdc, -2Vdc. The states of the switches have been summarized in Table 1. To increase the number of levels of the output voltage, the number of cells that is the Cell-1 is repeated for each additional level. The Fig.3 below shows the simulated results of the switching pulses generated for the studied five-level inverter. These are exactly the same switching pulses required for the studied five-level inverter employing the phase disposition PWM technique as represented in Fig. 2.

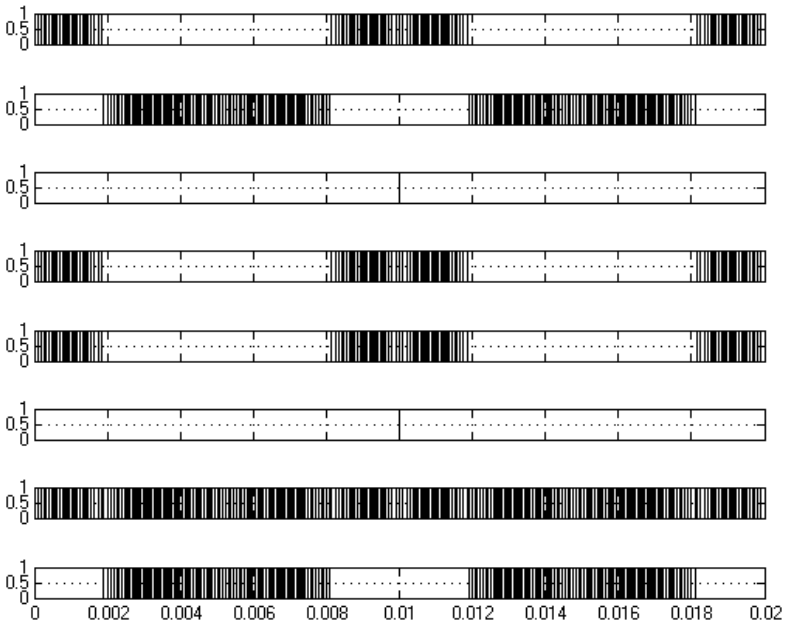

Fig. 3. Switching Pulses for the Six Switches of the Five-Level Inverter.

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The signals C_A and C_B, shown in Fig. 2, result from comparing the modulation waveform with the lower and upper triangle carriers, respectively. The switches Q1 and Q4 are operating at fundamental frequency, whereas the remaining switches such as Q2, Q3, S11 and S12 are operated at the switching frequency of 10 kHz. Here the modulation sinusoidal is having a fundamental frequency of 50 Hz, so that the time period is 0.02s. Hence all the simulation results presented here are simulated for a time period of 0.02s.

IV. SIMULATION RESULTS

The Fig.4 shows the output voltage and current waveforms of the studied single-phase five-level inverter under open loop configuration. The five-level output voltages obtained here are 2Vdc, Vdc, 0, -Vdc, -2Vdc. The current magnitude is about 10 A without any usage of filter but it is sinusoidal in shape. Fig.5 shows the FFT analysis of the studied single-phase five-level inverter. This FFT analysis is done for the five-level output of the studied five-level inverter without a filter in open loop configuration. So that a THD level of 33.47% is occurring for an R-L load of 10Ω and 1mH.

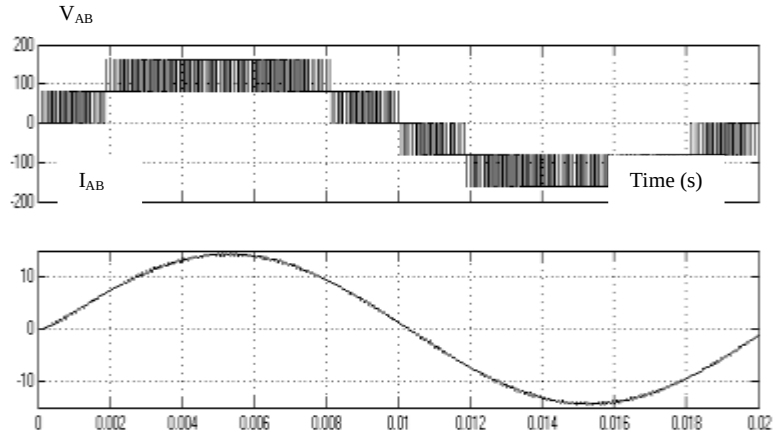

Fig. 4. Output Voltage and Current Waveforms for the Five-Level Inverter under Open-Loop Condition

But by introducing a L filter to the output side of the inverter, then the THD level can be decreased. This THD level can further be decreased by employing a PI current control.

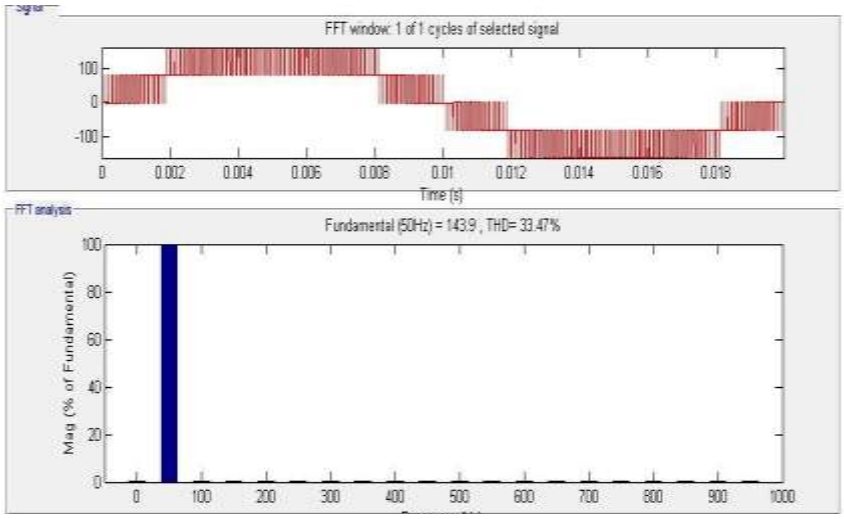

Fig. 5. FFT Analysis of the Studied Five-Level Inverter (Open-Loop)

The feedback controller used in this application uses the basic current control loop that equipped with PI controller as shown in Fig. 6.The actual grid current is detected and compared with the reference grid current Iref using the comparator. The reference current Iref is generated from the detected grid voltage in order to ensure that the injected grid current is in phase with grid voltage and always operate at unity power factor. The instantaneous current error is fed to the PI controller. The resulting control signal u is compared with the two triangular carrier signals, and the

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intersections between them will produce PWM switching signals for the inverter switches. The control system has been implemented using DSPACE DS1103. An L filter is used to ensure sinusoidal injected grid current to minimize the total harmonic distortion (THD). The injected current to the grid must meet the standard limit of the THD [13].

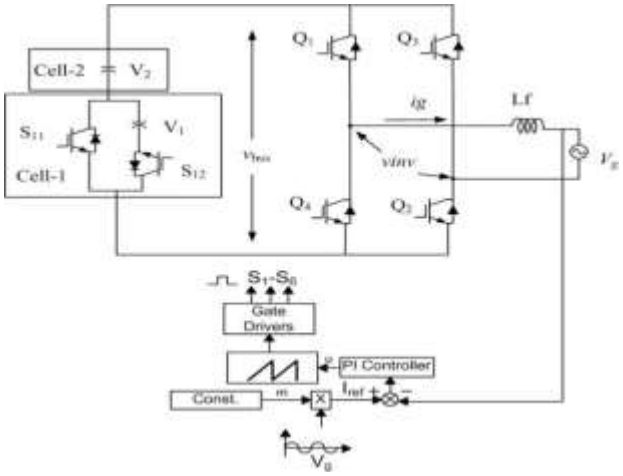

Fig. 6. Single-Phase Five-Level Grid-Connected Inverter with PI Control

Now for two different RL loads the simulation is carried out employing PI control. The inverter current THD and the grid current THD are measured for two different load conditions. The aim behind using the PI control is to minimise the THD within the standard limits specified by the IEEE 519. The in-phase current injection and current sharing are the two main tasks performed by this grid connected five-level inverter. An L filter of 5 mH is used as the filter in order to make the five-level output of the inverter to a smoother sinusoidal wave. The main advantage of this grid connected inverter topology is the reduction in the filter size.

This PWM technique is carried out at various modulation index conditions (MI >1) (MI < 0.5), and (0.5 ≤ MI ≤ 1.0). It is cleared that when (MI < 0.5) Vinv is less than √2 Vg, it means the current will be injected from the grid into the inverter. Therefore this condition must be avoided to prevent reverse power that may damage the inverter. However, at MI >1 the reference signal exceed the maximum amplitude of the both carrier signals, which causes the inverter to work at over modulation and saturation condition This also causes grid current to have a flat portion at the peak of the sine waveform, and hence it will not be pure sinusoidal waveform. In order to confirm the power transfer from DC link to the grid, it is recommended to limit the modulation index to be within (0.5 ≤ MI ≤ 1.0). The inverter output voltage Vinv and grid current Ig for optimal operating condition. The studied system composes of single-phase five-level inverter connected to the utility grid.

If the output of this studied inverter is designed to inject current to the grid, then this PI control algorithm is so important so as to inject the current to the grid that will meet the standard limit of THD (5% as per IEEE 519 Standards).The switching frequency has been selected as 10 kHz. Two identical power supplies of 80 V were used for the dc bus (> √2 Vg; in this case, Vg is 100 Vrms) in order to inject current into the grid. The actual grid current, and reference grid current are compared and the corresponding waveform of the two signals are compared and the error signal is given to a PI controller inorder to generate the required switching pulses for the six switches of the grid-connected inverter under closed loop operation. The reference current is generated by feeding back the grid voltage and converting it in to per unit value using a PLL block in the simulink and then on multiplying it with a constant the required reference current is generated.

The constant is chosen such that the resultant signal from the PI Controller does not exceed the MI range between 0.5 and 1, or else the system will move on to over modulation resulting in improper switching, higher THD and larger filter size. The output of the PI Controller is then utilised in the logic circuit to produce the necessary switching signals for the six switches of the grid connected five-level inverter.

Case 1: RL Load: 1Ω, 0.5mH: Fig. 7 shows the simulation results of the grid connected five-level inverter for an RL load of 1Ω, 0.5mH. At this load, the inverter output voltage, the inverter current, the grid voltage, the grid current and the load current are all in phase. The load current is about 110A for a 100Vrms and load of 1Ω, 0.5mH. The inverter current magnitude is 6A and the remaining current is supplied by the grid itself.output voltage is obtained with output voltage levels at +100V,+50V,0V,-50V and -100V respectively.

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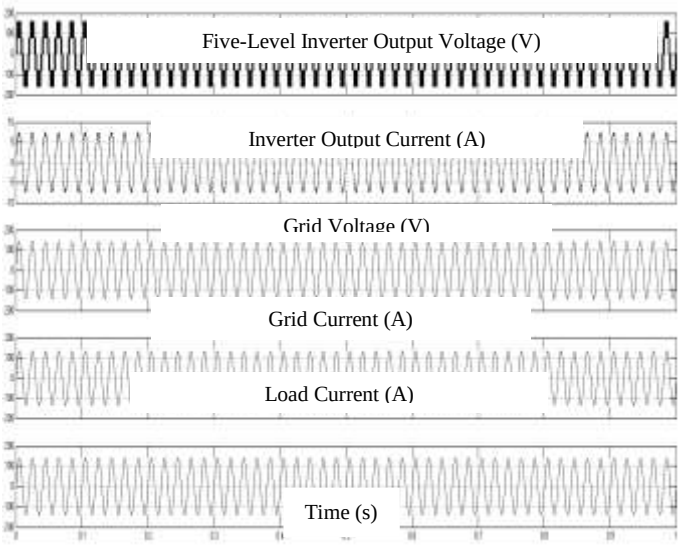

Fig. 7. Simulated Waveforms of a) Five-level output voltage b) Inverter Current c) Grid Voltage d) Grid Current e)Load Current

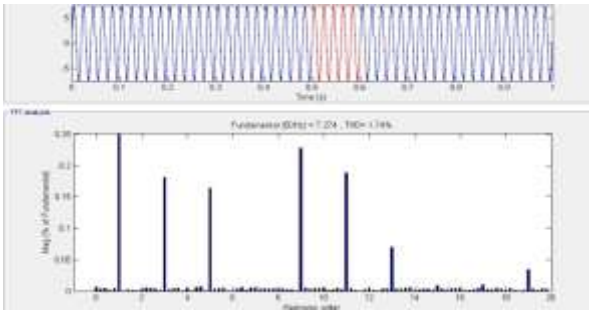

Fig. 8. FFT Analysis of the Studied Five-Level Inverter for Inverter Output Current

Fig. 8 shows the FFT analysis of inverter output current and the THD is obtained as 1.74%.

Case 2: RL Load: 100Ω, 15mH: The Fig. 9 shows the simulation results of the grid connected five-level inverter for an RL load of 100Ω, 15mH. At this load, the inverter output voltage, the inverter current, the grid voltage and the load current are all in phase. But the grid current is out of phase. The load current in this case is about 1A for a 100Vrms and load of 100Ω, 15mH. The inverter current magnitude is 6A and the inverter will provide the current required for the load and the remaining current is injected in to the grid and it is the reason for the grid current alone appearing as out of phase.

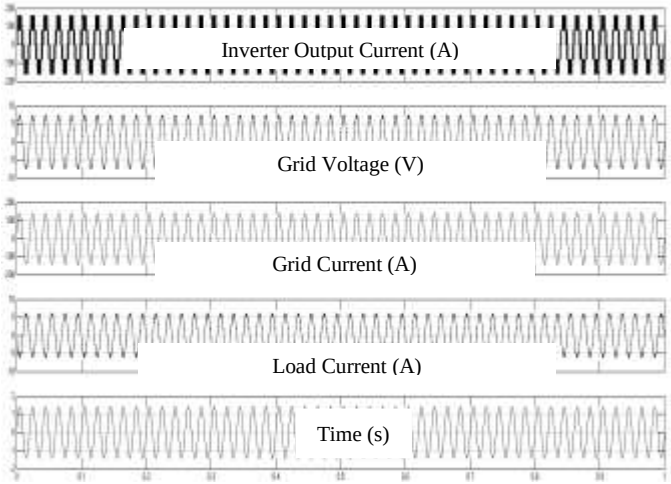

Fig. 9. Simulated Waveforms of a) Five-level output voltage b) Inverter Current c) Grid Voltage d) Grid Current e)Load Current

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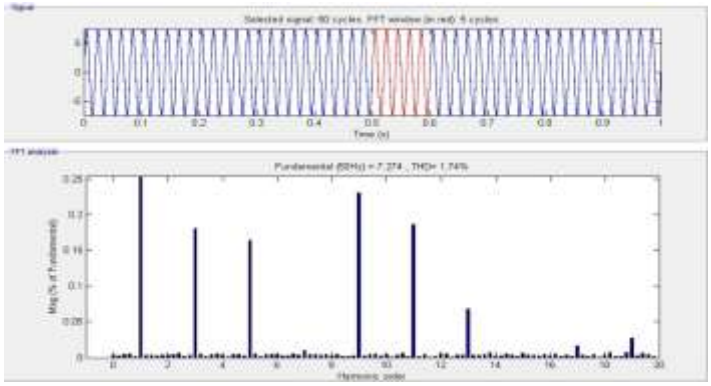

Fig. 10. FFT Analysis of the Studied Five-Level Inverter for Inverter Output Current

Fig. 10 shows the FFT analysis of inverter output current. The inverter current THD is obtained as 1.74%.

V.CONCLUSION

Industrial applications and utility application require medium voltage and high power levels. Basically, renewable energy sources for grid connected applications are increased due to the world energy crisis. Injecting power to the utility must meet the world harmonic standards. Here a grid-connected single-phase multilevel inverter is introduced with less number of elements compared with other single-phase inverter found in the literature. The load output voltage will have five states 2Vdc, Vdc, 0, -Vdc, -2Vdc. . It uses two carrier signals to generate PWM signals for the switches. It has less number of power elements. Some switches operate at fundamental load frequency and others operate at carrier frequency. The advantages of the studied inverter are smaller filter size, less circuit layout complexity and high efficiency.

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BIOGRAPHY

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